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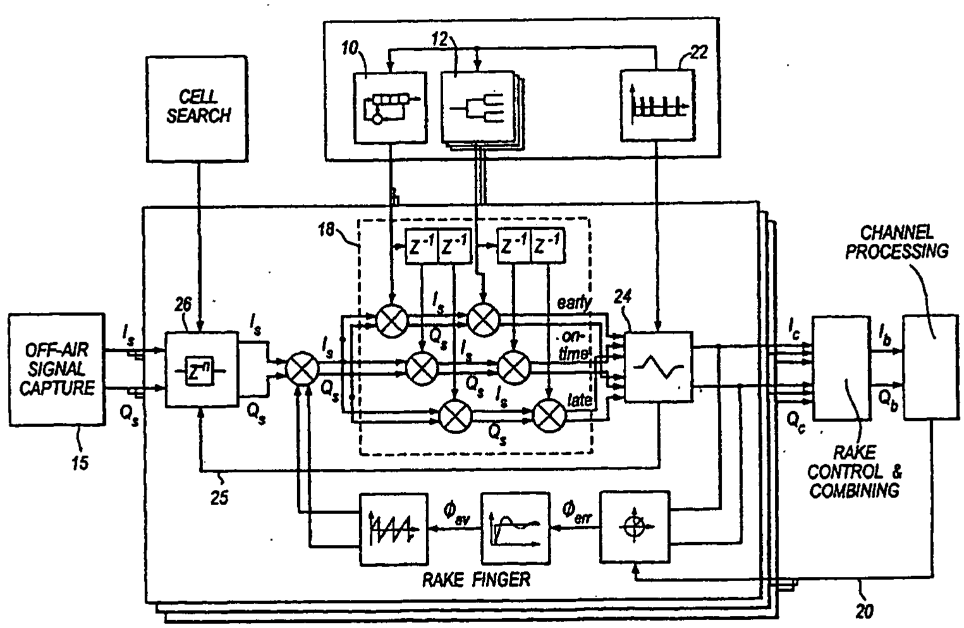

(57) Abstract

Circuitry for direct-sequence spread-spectrum receiver function to synchronise a locally generated code sequence with a received signal by generating the local code at a fixed rate while applying a variable delay to the received signal to achieve synchronisation. This arrangement simplifies the means generating the local code as it can simply run at a fixed rate.

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CODE TRACKING LOOP FOR A SPREAD-SPECTRUM RECEIVER

TECHNICAL FIELD OF THE INVENTION

The present invention relates to the generation of pseudo-random binary sequences (PRBS), or pseudo-noise (PN), for use as the de-spreading codes in a direct-sequence spread-spectrum (DS-SS) receiver in a DS-SS communications system.

More particularly, the present invention presents a new form of code generation tracking loop and an associated method of code tracking which can be used to align and synchronise the received pseudo-noise waveform with the generated PN code sequence to allow the received PN waveform to be de-spread into the required information signal. The tracking loop of the present invention is particularly suitable for use in DS-SS receivers with a RAKE architecture to compensate for multi-path signal propagation.

DESCRIPTION OF THE PRIOR ART

Spread spectrum communications techniques such as direct sequence spread spectrum (DS-SS) and frequency -hopping spread spectrum (FH-SS) have been popular in various military applications for many years, primarily due to the increased communications security that such arrangements provide. In recent years, however, direct sequence spread spectrum techniques have also been considered for various civil and commercial uses, most notably within the field of mobile communications based on code division multiple access (CDMA). DS-SS is particularly attractive for use within this application because of its inherent capabilities to mitigate the interference effects of, for example, multi-path signal propagation, simultaneous multi-user access, multiple cell sites, and multiple media.

The basic operational characteristics of a DS-SS system are well known in the art, but for completeness the following brief overview is provided.

Within a DS-SS system, a baseband bit stream of data rate $1/T_b$

representing the information to be transmitted is multiplied by a pseudo-random binary sequence of clock period T_c (the *chip* period), wherein $T_b >> T_c$. This has the effect of increasing the bandwidth of the signal by the ratio of T_b / T_c. This spread signal is then transmitted over the wider band with a reduced power spectral density (PSD) relative to a corresponding de-spread signal.

At the DS-SS receiver, the received wide-band spread spectrum signal must be de-spread in order for the information data to be recovered. De-spreading is achieved by multiplying the spread signal by an exact replica of the PRBS modulation sequence used in the transmitter. This has the dual effect of not only de-spreading the required signal (with a corresponding increase in PSD), but also of spreading any interference introduced into the received signal by the channel. Thus spread spectrum systems characteristically possess a degree of noise rejection which can make them more attractive over other communications systems.

As stated, in order for correct de-spreading, the received PN waveform must be multiplied by an exact replica of the PRBS spreading code, the replica being in exact synchronisation and alignment to the received PN waveform. There are thus a multitude of tasks that a practical DS receiver must perform. In particular, the receiver must first acquire the PN waveform. That is, the local PRBS generator that generates the PN waveform at the receiver used for de-spreading must be aligned and synchronised to within one chip of the received PN waveform.

Code synchronization is usually performed in two stages: initial coarse code acquisition and then followed by fine code tracking. Coarse code acquisition typically reduces the alignment timing offset between a received PN waveform and the locally generated de-spreading code to less than a chip period. Code tracking then aligns, and maintains the alignment, of the two sequences to sub-chip precision.

In Third Generation (3G) mobile systems employing DS-SS, coarse

code acquisition can be achieved using a Cell Search hardware module, such as described in ETSI Document, UMTS XX.07 v 1.0 (1998-09), UTRA Layer 1 Description, Physical Layer Procedures, Section 5, pp 7-8. Code tracking can then be performed using a separate tracking loop. Popular tracking loops used previously are delay-locked loops for time-continuous systems, or its time-multiplexed version the tau-dither loop. A delay-locked loop of the prior art is shown in Figure 1, implemented within a RAKE Receiver hardware module of a form such as that previously described in "Microcellular Direct-Sequence Spread-Spectrum Radio System Using N-path RAKE Receiver", IEEE Journal on Selected Areas in Communications Vol. 8, No. 5, June 1990 pp 774-777, U. Grob et al. It must be noted that Figure 1 shows a full schematic of a whole RAKE finger, of which the Delay Lock Loop forms but a part. The following description therefore refers only to those functional blocks on Figure 1 which comprise the Delay Lock Loop.

With reference to Figure 1, a Delay Lock Loop (DLL) is a closed loop controller comprising a phase detector, a loop filter, and a numerically controlled oscillator, and is used to adjust the code generation rate of a local PRBS code generator to match the apparent rate of the same code in a received PN waveform.

The phase detector estimates the code phase error over a variable chip period , normally by comparing the received signal with time shifted replicas of the locally generated reference code sequence. The phase detector is contained within the functional block labelled 'EL code delay detector' 2 in Figure 1

The loop filter is arranged to receive the output from the phase detector and is required to smooth the output of the detector to make it robust to noise and considerate of inherent delays in the DLL. The loop filter is also contained within the functional block labelled 'EL code delay detector' 2 in Figure 1.

The numerically controlled oscillator (NCO) 4 (labelled 'variable

rate code clocks' in Figure 1) is arranged to receive the filtered output from the loop filter by means of a control line 6. The NCO then increases or decreases the time period between each pulse it produces in response to this received signal to act as a controlled variable rate clock for the code generator (i.e. it contracts or expands the clock period). The produced variable bit rate clock is then fed to the channel code generator 12 and the scramble code generator 10 to control production of the local PN sequence. A separate clock 4 and set of code generators 10 and 12 must be provided for every single RAKE finger, even though several of the receiver fingers may be assigned to track the same signal. Once generated, the code sequence for a particular receiver finger is then multiplied with the received PN sequence in conventional de-spreading means 18 to de-spread the received signal. Three branches of multiplications are made, each subsequent branch with an increasingly delayed copy of the generated PN sequence, to correspond to early, on-time, and late receipt of the PN waveform with respect to the generated local PN sequence. The three de-spread signals are then fed to the Early-Late Code detector for detection of phase error, and to close the delay-locked loop. In the particular RAKE implementation shown, the prior art uses an individual variable delay line 14 which is positioned inside of the data-directed frequency and phase locked loop (F&PLL) 20, and is implemented separately for each RAKE receiver finger. Each individual delay line must be long enough to cope with whatever relative delay changes occur between that particular signal path and the other multi paths since their role is to maintain the time-alignment of each of the outputs from the RAKE receiver fingers.

The prior art as described therefore provides a DS-SS receiver using a delay-locked loop, wherein the generation of the local PN sequence is controlled by means of a closed loop about a variable bit rate clock. The clock rate is controlled to match the rate of code generation to the rate at which the received PN waveform is received. Furthermore, in the particular RAKE implementation described and shown in Figure 1, separate variable delays must be provided within

the RAKE F&PLL to maintain the time alignment between the individual outputs from each of the RAKE fingers assigned to track the same received PN waveform signal.

In addition to the above described delay lock loop used for code tracking, a further code acquisition circuit is described in GB 2315647 (Roke Manor Research). Herein a variable delay operates to introduce a delay shift into the received spread spectrum signal, the delay introduced being a random fraction m/M of a chip. The delays introduced are therefore always less than 1 chip, and the design fundamentally runs at chip rate. Following delay, the received signal is de-spread and a correlation is performed which operates to correlate n-chips of the local reference code with n-samples of the received signal. The result of the correlation is used to maintain the delay shift for at least one correlation, and to determine whether the delay applied to the received signal should be changed. When it is decided that the delay should be changed, a new random delay is applied, generated by a random number generator. The delay applied to the received signal is not controlled in a closed-loop fashion, and code tracking is not therefore possible.

SUMMARY OF THE INVENTION

In contrast to all of the above, the present invention presents a novel code tracking loop which may be used instead of a delay-lock-loop in a DS-SS receiver, and which is termed a lag-lock-loop (LLL) herein. Instead of matching the rate of local PN code generation to the actual receipt rate of a received PN waveform as in a DLL, the LLL of the present invention instead adjusts the apparent receipt rate of the received PN waveform to match the fixed rate of a local PN code generator. Such an arrangement presents many advantages over the prior art DLL arrangement, and which will become apparent from the later detailed description of a specific embodiment thereof.

According to the present invention there is provided a circuit means for code tracking and alignment in a direct-sequence spread-spectrum receiver,

comprising:

variable delay means arranged to receive a received spread-spectrum signal and to apply a variable time delay to said received signal in response to delay control signal;

code generation means arranged to generate a local de-spreading code at a fixed rate;

de-spreading means arranged to receive said received signal from said variable delay means and to receive said local fixed-rate de-spreading code from said code generation means, and to produce a plurality of de-spread signals therefrom, each of said plurality of de-spread signals being time-shifted with respect to the others;

code phase detector means arranged to receive said plurality of de-spread signals and to determine a code phase error between the received spread-spectrum signal and the local fixed rate de-spreading code therefrom; and

delay control means arranged to receive said code phase error from said code phase detector means and to use said code phase error to produce the delay control signal for said variable delay means;

wherein said variable delay means delays the received spread-spectrum signal so that an apparent receipt rate of the received spread-spectrum signal is the same as the fixed rate at which the local de-spreading code is generated whereby the received spread-spectrum signal is maintained in alignment with the local de-spreading code.

According to another aspect of the present invention, there is also provided a method of code tracking and alignment for use in a direct-sequence spread-spectrum receiver, comprising the steps of:

a) delaying a received spread-spectrum signal by a variable time delay;
b) generating a local de-spreading code at a fixed rate;
c) de-spreading the received spread-spectrum signal using the local fixed-rate de-spreading code to produce a plurality of

de-spread signals, each of said plurality of de-spread signals being time-shifted with respect to each other;

d) detecting a code phase error between the local fixed-rate de-spreading code and the received spread-spectrum signal using the plurality of de-spread signals; and

e) controlling said variable time delay of step a) on the basis of said code phase error;

wherein said variable time delay ensures that an apparent receipt rate of the received spread-spectrum signal is adjusted to be the same as the fixed rate at which the local de-spreading code is generated whereby the received spread-spectrum signal is maintained in alignment with the local de-spreading code.

The present invention can be implemented in any DS-SS receiver, but is particularly suitable for use in receivers employing a RAKE architecture.

It is an advantage of the present invention that the invention uses a fixed rate code clock, which is allowed to free run, rather than a variable rate clock under closed-loop control. The advantage arises because it is far easier to implement a free-running clock which produces pulses at a fixed rate, than a closed-loop controlled clock which produces pulses at a variable rate.

There is a further advantage of the present invention in that when the invention is used with a RAKE receiver architecture, the invention uses a common variable delay line which is positioned before the data-directed F&PLL, and is shared by each and every RAKE receiver finger. This means that the data-directed feedback path of the frequency and phase lock loop (F&PLL) has a delay lag which is fixed in length and shorter than is traditionally the case in the prior art. A shorter delay lag in the feedback path of a F&PLL means that the loop is capable of responding more quickly to changes of frequency and phase in the received signal. This is particularly important in an application such as mobile communications in which the radio propagation environment can change rapidly.

Furthermore, again where a RAKE receiver architecture is adopted,

there is a further advantage in that the same scrambling code generator can be used for all RAKE receiver fingers that are assigned to track the same signal, because they will all use the same phase of the code. As only one, rather than several, code generators need to run per tracked signal, overall power consumption will be reduced.

DESCRIPTION OF THE DRAWINGS

Further features and advantages of the present invention will become apparent from the following detailed description of a particularly preferred embodiment thereof, and with reference to the accompanying drawings, in which like parts are referred to with like numerals, and in which:-

Figure 1 shows a schematic of a known delay lock loop arrangement used for code tracking in a DS-SS RAKE receiver of the prior art;

Figure 2 shows a schematic of a lag lock loop of the present invention implemented in a DS-SS RAKE receiver;

Figure 3 shows a schematic of a code delay detector used in the lag lock loop of the present invention; and

Figure 4 shows a schematic block diagram of a variable delay means for use in the lag lock loop of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In this invention circuitry, termed herein "Lag Lock Loop", is a direct-sequence spread-spectrum receiver which functions to synchronise a locally generated code sequence with a received signal by generating the local code at a fixed rate while applying a variable delay to the received signal to achieve synchronisation. This arrangement simplifies the means generating the local code as it can simply run at a fixed rate.

With reference to Figures 2, 3, and 4, a Lag Lock Loop is a closed loop controller, which has three basic parts.

Firstly, a phase detector is provided which estimates the code phase error between the received PN waveform and locally generated reference PN

sequence over a fixed chip period by comparing the received signal with time shifted replicas of the locally generated reference code sequence. This phase detector forms part of the functional block labelled 'EL code delay detector' 24 in Figure 2, and its functional parts are shown in greater detail in Figure 3. The operation of the EL delay detector 24 will be described in detail later.

Secondly, a loop filter is provided which is arranged to receive the output from the phase detector, and which is required to smooth the output of the detector to make it robust to noise and considerate of inherent delays in the LLL. This is also included as part of 'EL code delay detector' 24 of Figure 2, and is shown as LPF 31 in Figure 3.

Finally, a controlled variable delay line 26 is arranged to receive a control signal from the Early-Late code delay detector 24 via a control line 25. The variable delay 26 is placed before the de-spreading means 18 so that the delay may be applied before the received signal is de-spread. The output of the de-spreading means 18 is fed to the Early-Late Code delay detector 24 so as to close the LLL. The variable delay line 26 must be long enough to accommodate the delay spread of a signal affected by multipath propagation, and its role is to maintain the time-alignment of the input to the RAKE receiver fingers.

At least one code generation means comprising a scrambling code generator 10, a channel code generator 12 and a fixed rate code clock 22 is provided, and which is shared between all RAKE fingers when a RAKE receiver architecture is adopted. The fixed rate clock 22 is arranged to provide a fixed clock to the EL code detector 24, and to the code generators 10 and 12. The code generators each respectively provide the required de-spreading codes to the de-spreading means 18 at a fixed rate. The same de-spreading codes may be supplied to all RAKE fingers assigned to track the same signal, as they will all use the same phase of code. This is because the control signal from the EL code delay detector to the variable delay is used to control the variable delay so as to increase or decrease a time delay applied to the received PN waveform before it is processed

(i.e. it expands or contracts the period of each datum) so as to synchronise the apparent receipt rate of the received PN waveform with the fixed rate locally produced PN code sequence. This has the effect of aligning the received PN waveform to the local PN sequence to allow the received signal to be de-spread. By allowing an output to be taken from the variable delay at any one of several unit delay taps (32, Figure 3) then several RAKE fingers can be supplied at once whilst still allowing for fading multi-path propagation delays.

Furthermore, by positioning the variable delay 26 prior to the de-spreading means 18 and out of the frequency and phase lock loop 20 then the F&PLL delay lag becomes fixed in length and shorter than in the prior art case wherein unknown demodulated data are fed back. More particularly, without the variable delay in the loop, the F&PLL has a delay lag which is fixed and the same as traditionally the case when known pilot data are fed back. This is an important advantage as a system will typically spend more time carrying unknown data than pilot data, since the former bears the information content. Any decrease in delay lag of the loop will mean that the loop is capable of responding more quickly to changes of frequency and phase of the received signal, as can happen often in the mobile radio propagation environment.

The detailed method of operation of a LLL of the present invention will now be described.

An analogue-to-digital converter (ADC) 15 provides discrete-time complex samples of a received signal. The samples are loaded into a delay line 31 (Figure 4) of the variable delay means 26. The delay line 31 allows an output to be taken at any unit-delay tap 32, each output being fed to a multiplexer 42 arranged to be controlled by a counter 44. The value of the counter is determined by the control signal on the control line 25 from the Early Late Code Delay Detector 24. The index of the actual unit-delay tap output from the multiplexer 42 is determined by the current value of the counter 44.

Three copies (Figure 3) of the present output from the delay line 26

are taken and multiplied respectively by early, on-time and late replicas of the local scrambling and spreading codes in the de-spreading means 18. The three branches 30 are then each fed to the Early-Late Code delay detector 24, wherein further respective delays 32 are applied to the three lines as appropriate to achieve synchronisation of the three lines. More precisely, no delay is applied to the late signal, one unit delay is applied to the on-time signal, and two unit delays are applied to the early signal. The three synchronous signals are then accumulated over, dumped at the end of, and held for the duration of each chip period by respective accumulate, dump and hold means 34 The respective outputs of the accumulate dump and hold means 34 are then fed to respective modulus means 36 where the modulus of each signal is taken. The output modulus of the early estimate is then fed as a first input to a subtracter 38, and the output modulus of the late estimate fed to the subtracter as a second input, wherein the late estimate modulus is subtracted from the early estimate modulus. The resultant early-late difference is then fed to a first low pass filter 31. The output of the on-time modulus is fed directly to a second low-pass filter 31. The respective outputs of the filters are then fed to a divider 33 wherein the filtered early-late difference is divided by the filtered on-time estimate to normalise it.

The normalised value is fed to a threshold detector means 35 wherein it is compared with a pair of thresholds to produce the control signal 25 used to control the counter 44 of the variable delay. If the normalised value is greater than the upper threshold then a down instruction is generated as the control signal 25 to decrement the counter, if it is less than the lower threshold then an up instruction is generated as the control signal 25 to increment the counter, otherwise a hold instruction is generated as the control signal 25 to leave the counter unchanged. These instructions are issued unchanged to the counter, except where the aggregate effect of the instructions over some previous defined period would cause the counter to perform either a multiple increment, or a multiple decrement in that period. In these cases a hold instruction is issued. This is done

so the effect of a change in the counter can propagate through the LLL before another change in the same sense is allowed. This propagation delay is due to the processes of accumulation and alignment of the early, on-time, and late estimates.

When the counter is incremented or decremented the NCO 17 of the F&PLL 20 should be adjusted to wind-in or take-out one sample's worth of phase change due to any frequency offset of the signal carrier. The value held on the counter provides the index of the unit-delay tap from which the output of the delay line (holding the received signal samples) is taken, and so closes the feedback path of the LLL.

As will be apparent from the above, the present invention over samples the incoming signal by S, delays the incoming signal by t (where t could be much greater than S), and then uses every sample (ie. a stream of samples at S × chip rate.

The delays introduced can be significantly more than 1 chip, and the circuit means fundamentally runs at S × chip rate.

With respect to the variable delay t, the present invention uses a variable delay block, in which the size of the delay is set to a controlled amount for each symbol period to maintain synchronisation which has already been achieved. The control signal for the variable delay block is derived from the early/on-time/late discriminator block, and causes the delay to be incremented by one sample period, remain unchanged, or be decremented by one sample period as appropriate. In this way, because the delay can be controlled as finely as one sample period, sub-chip delay precision can be obtained thus allowing accurate code tracking.

CLAIMS:

1. A circuit means for code tracking and alignment in a direct-sequence spread-spectrum receiver, comprising:

variable delay means arranged to receive a received spread-spectrum signal and to apply a variable time delay to said received signal in response to delay control signal;

code generation means arranged to generate a local de-spreading code at a fixed rate;

de-spreading means arranged to receive said received signal from said variable delay means and to receive said local fixed-rate de-spreading code from said code generation means, and to produce a plurality of de-spread signals therefrom, each of said plurality of de-spread signals being time-shifted with respect to the others;

code phase detector means arranged to receive said plurality of de-spread signals and to determine a code phase error between the received spread-spectrum signal and the local fixed rate de-spreading code; and

delay control means arranged to receive said code phase error from said code phase detector means and to use said code phase error to produce the delay control signal for said variable delay means;

wherein said variable delay means delays the received spread-spectrum signal so that an apparent receipt rate of the received spread-spectrum signal is the same as the fixed rate at which the local de-spreading code is generated whereby the received spread-spectrum signal is maintained in alignment with the local de-spreading code.

2. A circuit means according to claim 1, wherein said direct-sequence spread-spectrum receiver is a RAKE receiver having one or more receiver fingers.

3. A circuit means according to claim 2, wherein said variable delay means is shared in common between those receiver fingers assigned to track the same received spread-spectrum signal.

4. A circuit means according to claims 2 or 3, wherein said code generation means is common to those receiver fingers assigned to track the same received spread-spectrum signal.

5. A circuit means according to any of the preceding claims, wherein said variable delay means further comprise:

one or more sequential unit-delay taps, arranged to receive the received spread-spectrum signal and to each apply a unit-time delay to said signal;

counter means arranged to receive the delay control signal; and

multiplexer means arranged to respectively receive successively delayed replicas of the received spread-spectrum signal from each of said sequential unit-delay taps, and to output a selected one of said delayed replicas according to a value held on said counter means;

wherein the value on said counter means is controlled by said delay control signal so that the received spread-spectrum signal is output from said variable delay means with a time-delay appropriate to maintain alignment with the local fixed rate de-spreading code.

6. A circuit means according to any of the preceding claims, wherein said code generation means further comprise:

a fixed rate clock; and

a de-spreading code generator arranged to generate a pseudo-random binary sequence identical to that used in a corresponding direct-sequence spread-spectrum transmitter to spread said received spread-spectrum signal;

wherein the pseudo-random binary sequence is produced at the fixed

rate according to said fixed rate clock.

7. A circuit means according to any of the preceding claims, wherein said de-spreading means further comprise:

a plurality of sequential unit-delay taps arranged to receive said fixed-rate local de-spreading code and to each apply a unit time-delay to said code; and

a plurality of multipliers, each arranged to receive the received spread-spectrum signal from the variable delay means, and each further arranged to respectively receive a time-delayed replica of the local de-spreading code from a different one of said sequential unit-delay tapes;

wherein each of said plurality of multipliers is arranged to multiply the received spread-spectrum signal with the respective one of said time-delayed replicas of the local de-spreading code whereby to produce said plurality of de-spread signals each being time-shifted with respect to the others.

8. A circuit means according to claim 1 or 7, wherein said plurality of de-spread signals correspond to an early signal, an on-time signal and a late signal.

9. A circuit means according to any of the preceding claims wherein said code phase detector means further includes a loop filter.

10. A circuit means according to any of the preceding claims, wherein delay control means further comprise thresholding means for comparing said code phase error with an upper and lower threshold value, and for generating said control signal dependent upon the result of said comparison.

11. A method of code tracking and alignment for use in a direct-sequence spread-spectrum receiver, comprising the steps of:

a) delaying a received spread-spectrum signal by a variable time delay;

b) generating a local de-spreading code at a fixed rate;

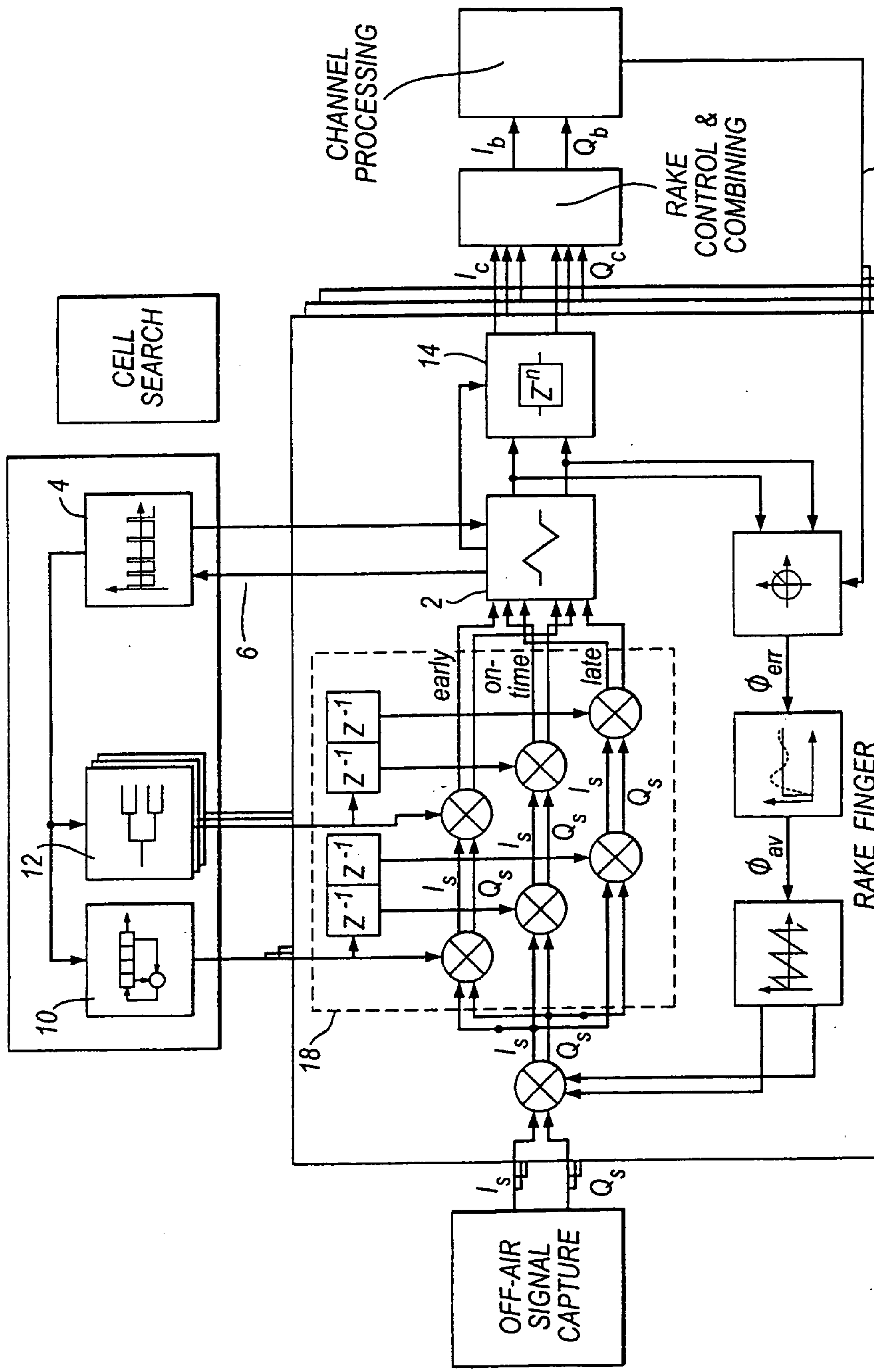
c) de-spreading the received spread-spectrum signal using the local fixed-rate de-spreading code to produce a plurality of de-spread signals, each of said plurality of de-spread signals being time-shifted with respect to each other;

d) detecting a code phase error between the local fixed-rate de-spreading code and the received spread-spectrum signal using the plurality of de-spread signals; and

e) controlling said variable time delay of step a) on the basis of said code phase error;

wherein said variable time delay ensures that an apparent receipt rate of the received spread-spectrum signal is adjusted to be the same as the fixed rate at which the local de-spreading code is generated whereby the received spread-spectrum signal is maintained in alignment with the local de-spreading code.

12. A method according to claim 11 wherein said direct sequence spread-spectrum receiver is a RAKE receiver.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RAKE CONTROL & COMBINING
CELL SEARCH
RAKE FINGER
OFF-AIR SIGNAL CAPTURE
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Fig.1

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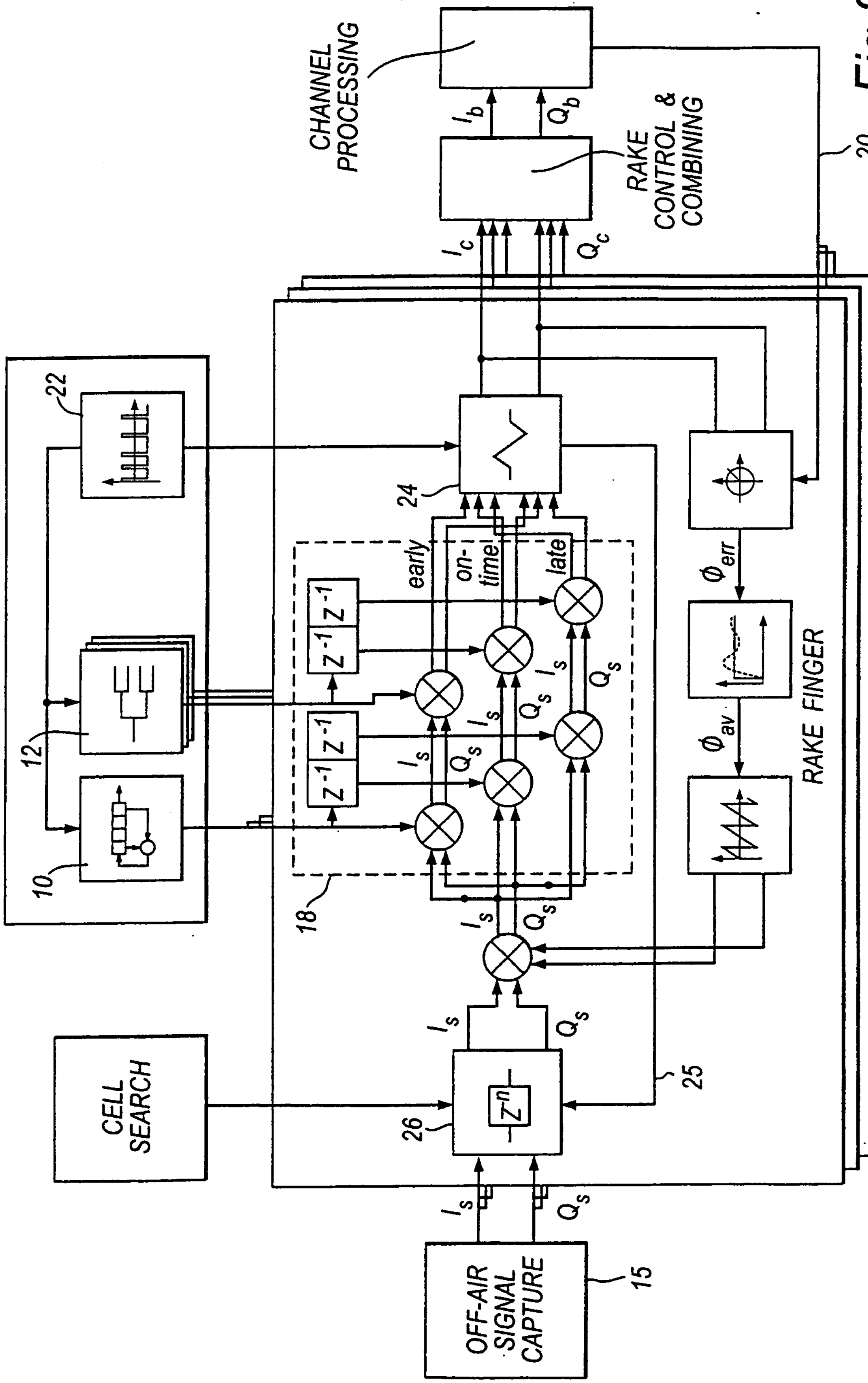
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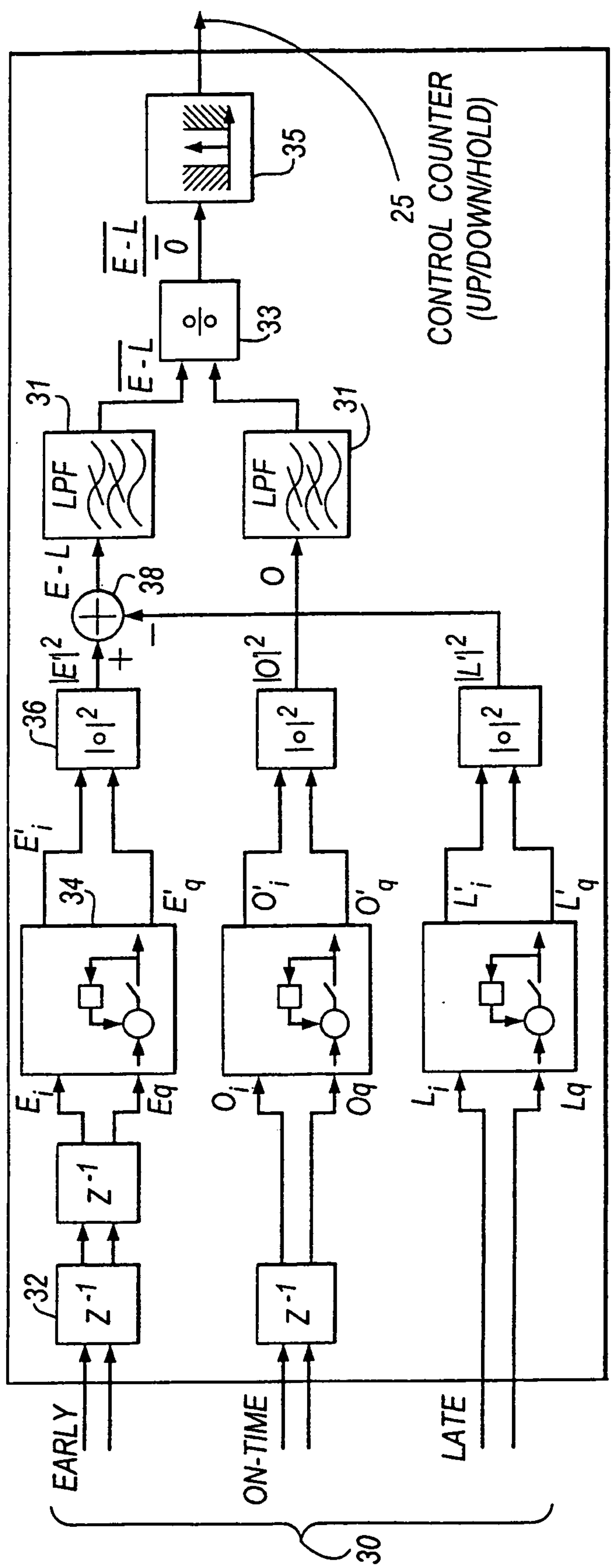
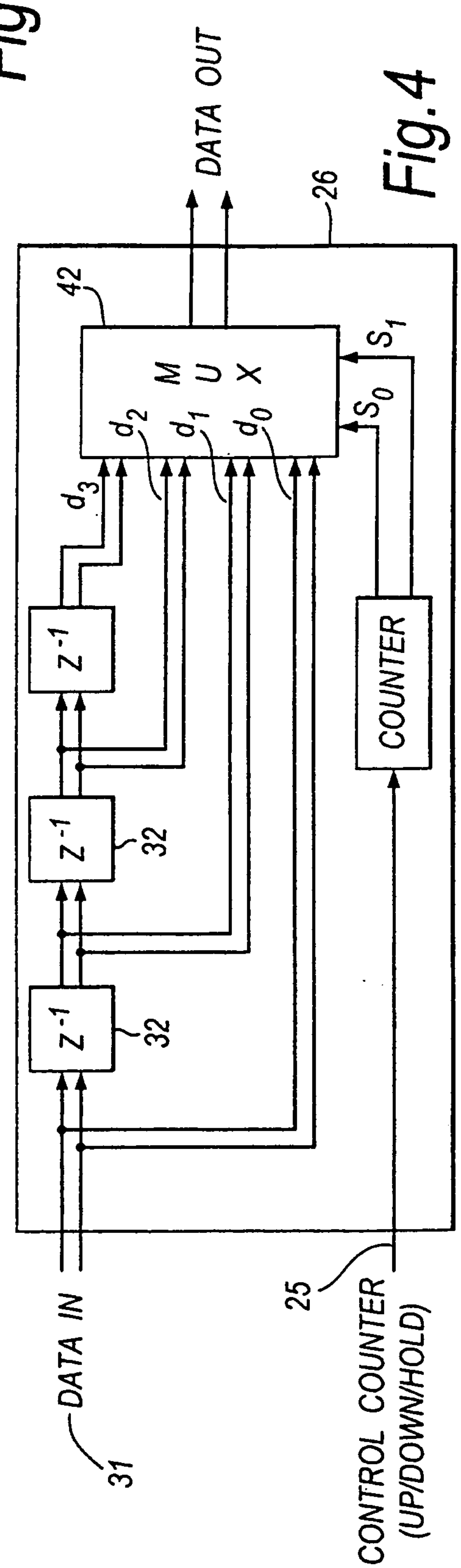
26

Fig.2



EARLY
ON-TIME
LATE
30
32
z^{-1}
E_i
Eq
O_i
Oq
L_i
Lq
34
E'_i
E'_q
O'_i
O'_q
L'_i
L'_q
36
$|\circ|^2$
$|E'|^2$
$|O|^2$
$|L'|^2$
+
−
38
E - L
O
LPF
31
$\overline{E-L}$
33
$\frac{\overline{E-L}}{\overline{O}}$
35
25
CONTROL COUNTER
(UP/DOWN/HOLD)

Fig.3



DATA IN
31
z^{-1}
32
d_3
d_2
d_1
d_0
M U X
42
S_0
S_1
COUNTER
DATA OUT
26
25
CONTROL COUNTER
(UP/DOWN/HOLD)

Fig.4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/04396

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 764 688 A (HULBERT ANTHONY PETER ET AL) 9 June 1998 (1998-06-09) column 1, line 44 - line 50 column 2, line 18 -column 3, line 40; figure 1	1-3,5, 7-9,11, 12
Y	US 5 029 181 A (ENDO AKIHIKO ET AL) 2 July 1991 (1991-07-02) column 1, line 24 - line 37; figure 2	1-3,5, 7-9,11, 12
A	EP 0 698 971 A (ROKE MANOR RESEARCH) 28 February 1996 (1996-02-28) page 4, column 5, line 26 -column 6, line 30; figure 4	1,2,11, 12

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2000	28/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bossen, M

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/04396

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 3048540 A	01-03-1991
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